

REMARKS/ARGUMENTS

Claims 1-5 and 36-53 are pending.

Claims 19-24 and 35 have been withdrawn from consideration as a consequence of a restriction requirement.

Claims 1-7, 34, and 36-40 were rejected under 35 U.S.C. Section 102 for allegedly being anticipated by Yokota et al. (U.S. Pat. No. 6,181,313).

Claim 1 recites storing information into a controller of a liquid crystal display that is sent from a device external to that controller. The information comprises a first number of original clock periods in a reference clock period and a second number of said reference clock periods in a scanning period. A frame frequency is determined based on the foregoing information. Yokota et al. disclose that a drive duty selection register (34) which contains a drive duty value that is used by the controller (2) to adjust the period of a shift clock signal of the timing signal generation circuit (10). *Col. 8, lines 45-49*. Yokota et al. further disclose that values in the drive duty selection register (34) are set by MPU (3). *Id at lines 43-45*. Based on the discussion at column 10, lines 16-37, the drive duty value takes on values such as $\frac{1}{2}$ and $\frac{1}{4}$. Yokota et al., therefore, do not show or suggest an external device sending the specific information of a first number of original clock periods in a reference clock period and a second number of said reference clock periods in a scanning period to the controller.

Claim 2 recites a control register having a first number of original clock periods and a second number of reference clock periods, where the first number and second number are received from a device external to the liquid crystal display controller. For the reasons set forth in the discussion above, Yokota et al. do not show or suggest this limitation of claim 2.

Claim 3 recites a control register for storing operating parameters received from a device external to the liquid crystal display controller. The operating parameters comprise a first number of reference clock periods in a scanning period, a second number of scan lines in a frame period, and a third number of original clock periods in said reference clock period. For the reasons set forth in the discussion above, Yokota et al. do not show or suggest this limitation of claim 3.

Claim 36 recites a first circuit for setting parameters for the display panel based on information received from an external device, where the parameters include a division ratio of an original clock signal and a number of clock of a reference clock signal per a scanning period. For the reasons set forth in the discussion above, Yokota et al. do not show or suggest this limitation of claim 36.

Claim 37 recites a first circuit for setting a division ratio of an original clock signal and number of clock of a reference clock signal per a scanning period based on information from an external device. For the reasons set forth in the discussion above, Yokota et al. do not show or suggest this limitation of claim 37.

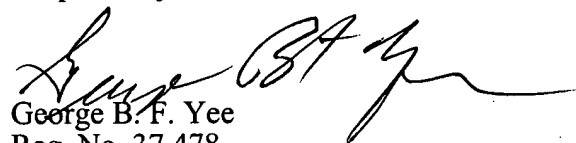
Claim 38 recites a register for setting a division ratio of the original clock signal and number of clock of a reference clock signal per a scanning period and a number of active lines of the display panel, all of which being received from a device that is external to the controlling device. For the reasons set forth in the discussion above, Yokota et al. do not show or suggest this limitation of claim 38.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,


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